

GA-MA770T-UD3P

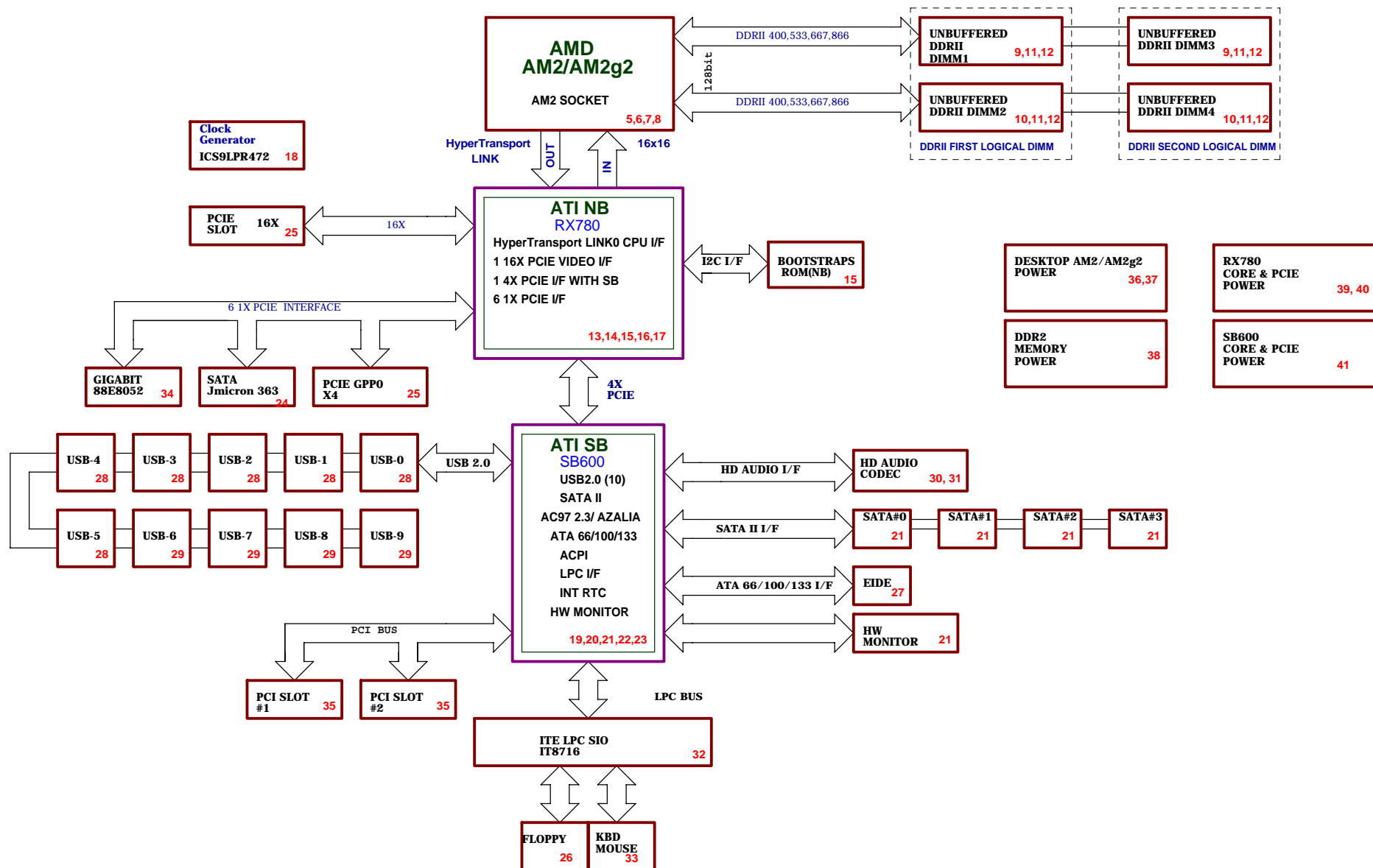
Revision : 1.1

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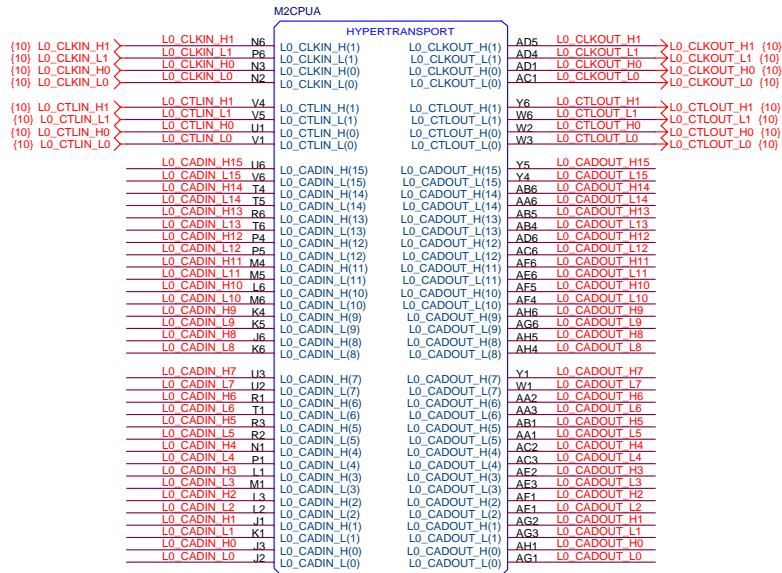
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# RX780 CUSTOMER DESKTOP REFERENCE DESIGN



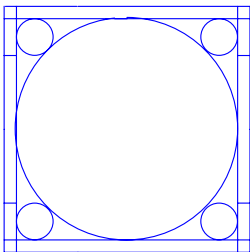
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L0\_CADIN\_H[0..15] <L0\_CADIN\_H[0..15] {10}  
L0\_CADOUT\_L[0..15] <L0\_CADOUT\_L[0..15] {10}  
L0\_CADOUT\_H[0..15] <L0\_CADOUT\_H[0..15] {10}



CPU\_VDD\_RUN = VCORE  
CPU\_VDDA\_RUN = VDDA25  
VLDT\_RUN = VCC12\_HT  
CPU\_VDDIO\_SUS = DDR15V  
CPU\_VDDR = CPU\_VDDR12

VLDT\_A = VCC12\_HT  
VLDT\_B = HT12B

M2CPU  
AM3RM/SC/BL/MB



GIGABYTE™

Title CPU HYPER TRANSPORT

Size Custom Document Number GA-MA770T-UD3P Rev 1.1

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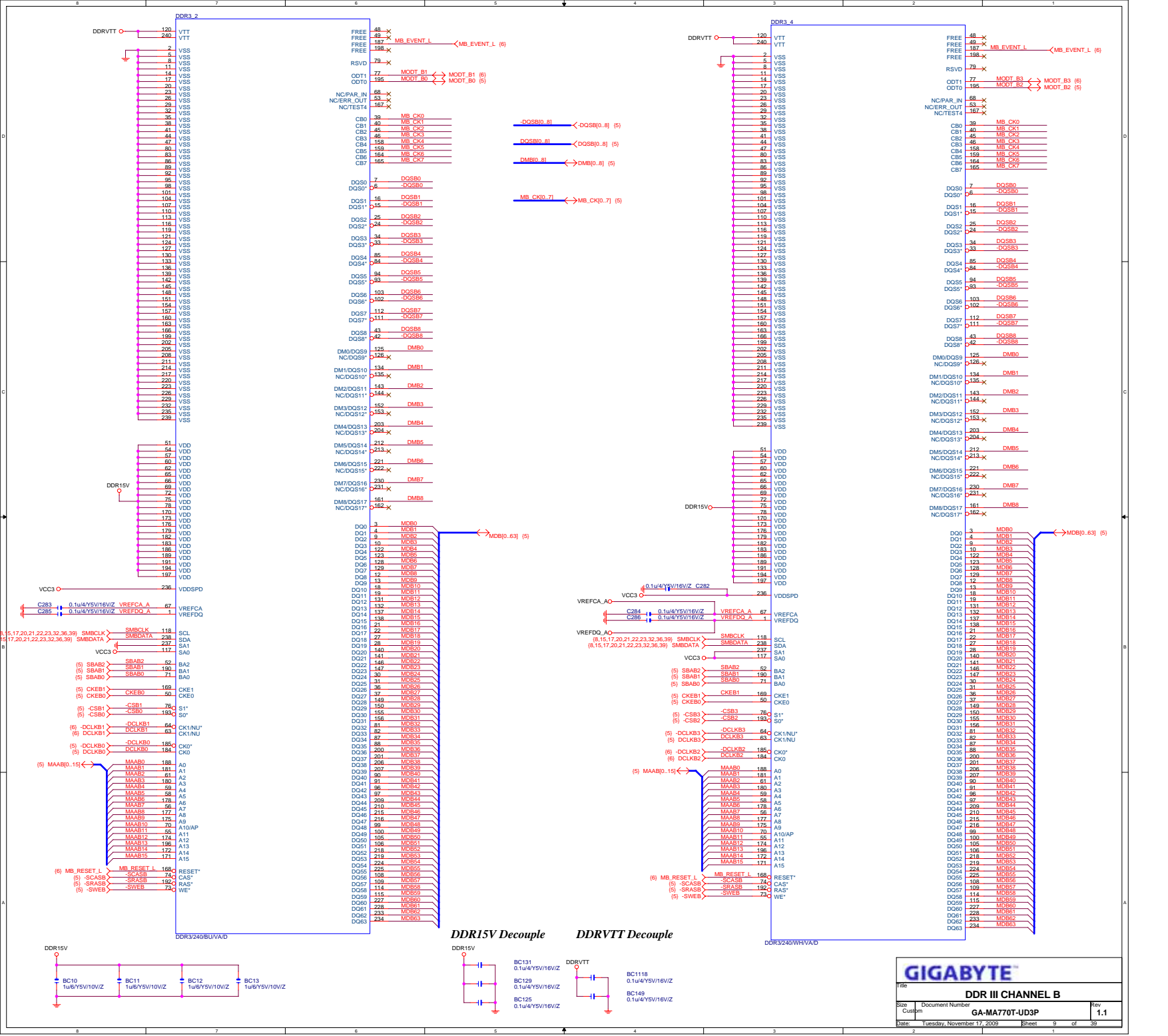












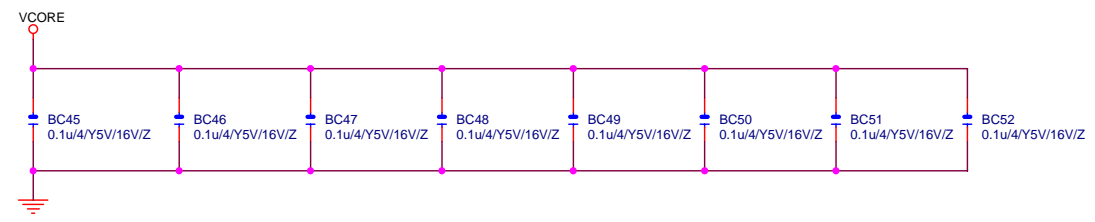
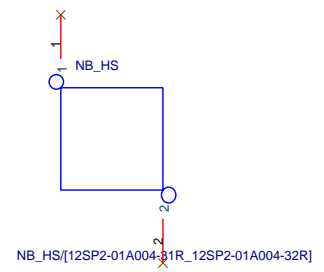


L0\_CADIN\_L[0..15] <L0\_CADIN\_L[0..15] (4)

L0\_CADIN\_H[0..15] <L0\_CADIN\_H[0..15] (4)

L0\_CADOUT\_L[0..15] <L0\_CADOUT\_L[0..15] (4)

L0\_CADOUT\_H[0..15] <L0\_CADOUT\_H[0..15] (4)



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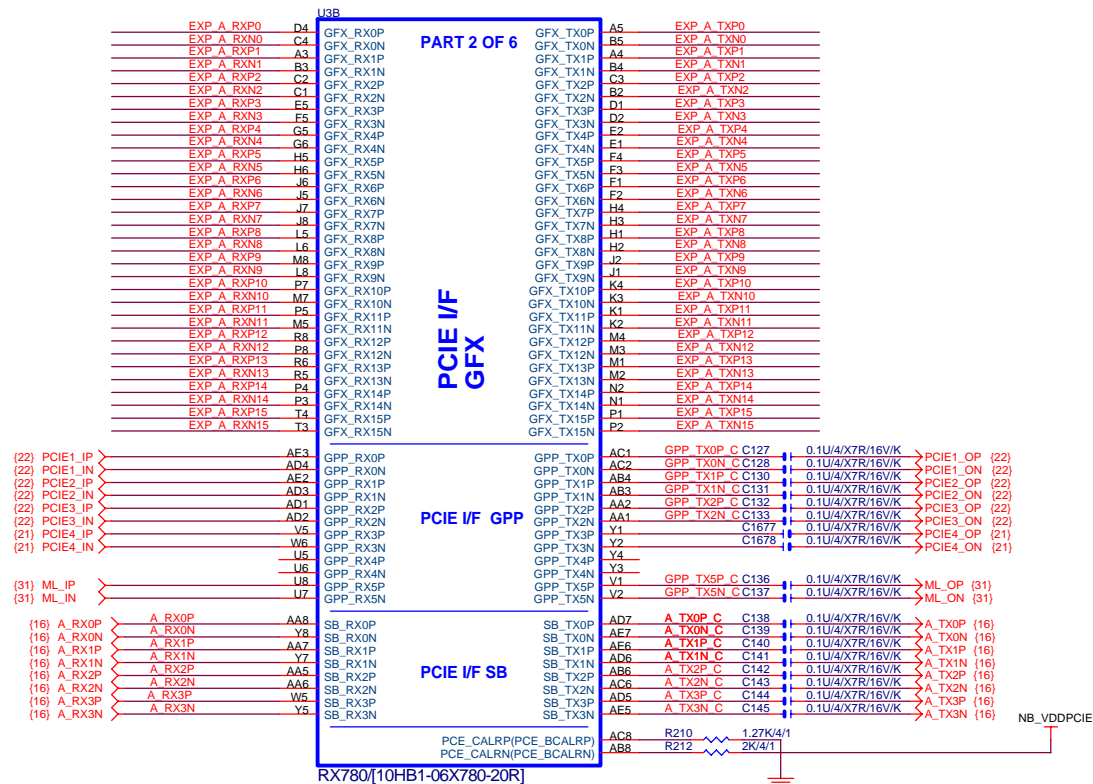
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RD780-HT LINK I/F

Size B Document Number  
GA-MA770T-UD3P

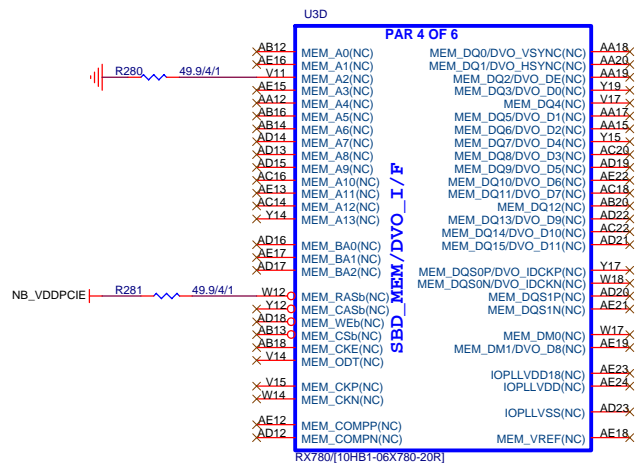
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Rev  
1.1

EXP A\_RXP0\_15I >>> EXP\_A\_RXP[0..15] (20) EXP A\_TXP0\_15I >>> EXP\_A\_TXP[0..15] (20)  
EXP A\_RXN0\_15I >>> EXP\_A\_RXN[0..15] (20) EXP A\_TXN0\_15I >>> EXP\_A\_TXN[0..15] (20)







#### DFT\_GPIO5: STRAP\_DEBUG\_BUS\_GPIO\_ENABLEb

Enables the Test Debug Bus using GPIO.  
1 : Disable ( Can still be enabled using  
nbcfg register access)  
0 : Enable

#### DFT\_GPIO[4:2]: STRAP\_PCIE\_GPP\_CFG[2:0]

These pin straps are used to configure PCI-E GPP mode.  
000 : 00001  
001 : 00010  
010 : 01011  
011 : 00100  
100 : 01010  
101 : 01100  
111 : 01011

#### DFT\_GPIO1: LOAD\_EEPROM\_STRAPS

Selects Loading of STRAPS from EPROM  
1 : Bypass the loading of EEPROM straps and use Hardware Default Values  
0 : I2C Master can load strap values from EEPROM if connected, or use  
default values if not connected

#### DFT\_GPIO0: STRAP\_DEBUG\_BUS\_PCIE\_ENABLEb

Enables the Test Debug Bus using PCIE bus  
1 : Disable ( Can still be enabled using nbcfg register access )  
0 : Enable

**GIGABYTE™**

Title

**RD780 STRAP**

Size

Document Number

**GA-MA770T-UD3P**

Rev

**1.1**

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Sheet

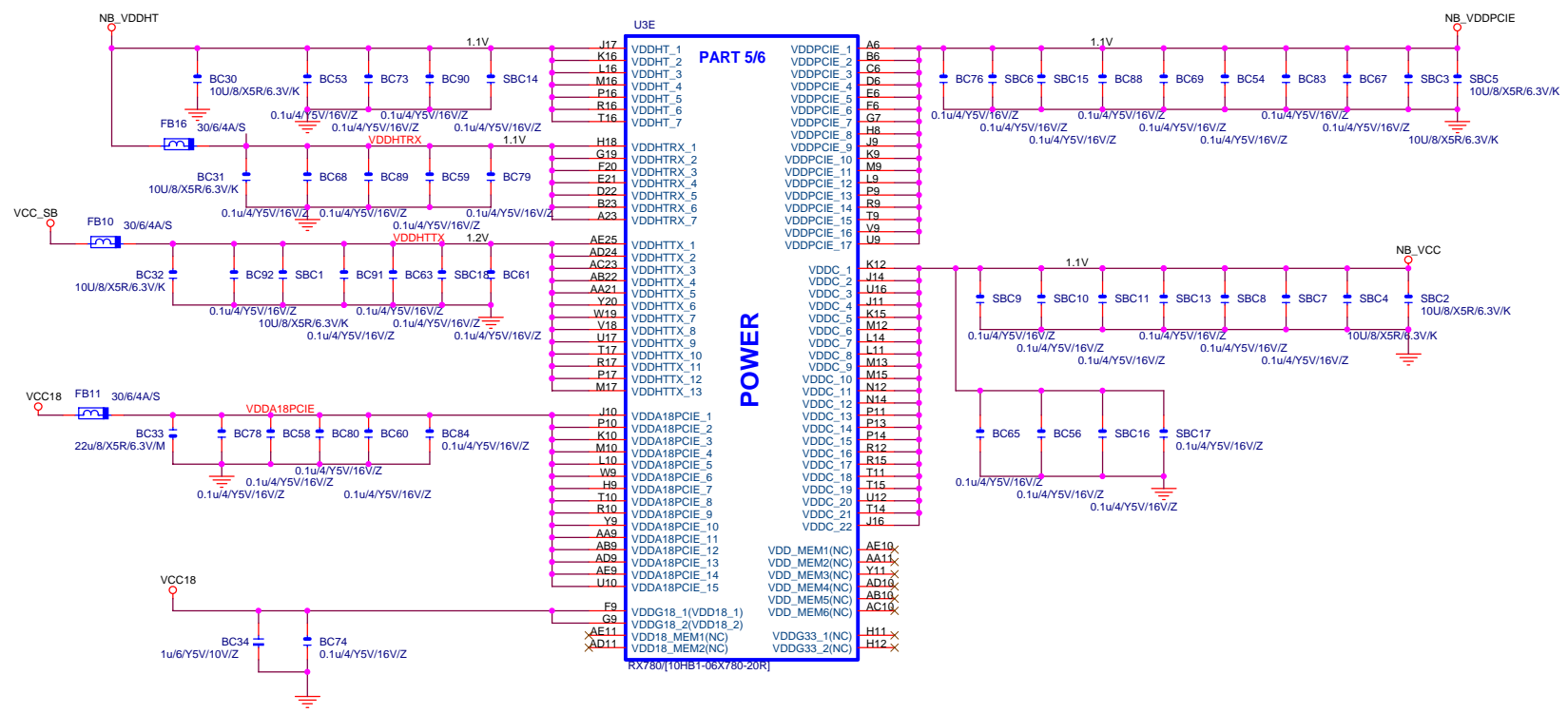
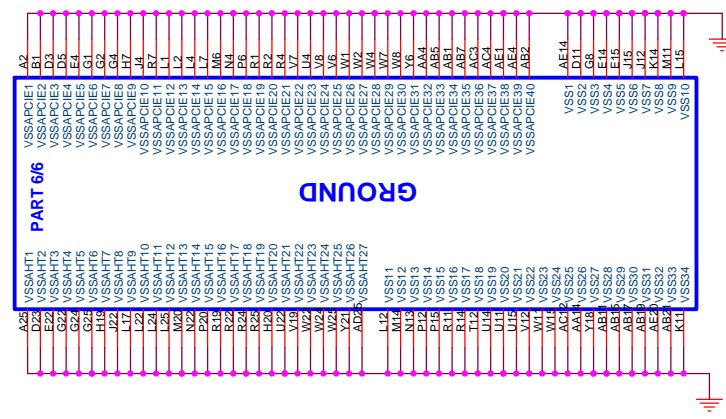
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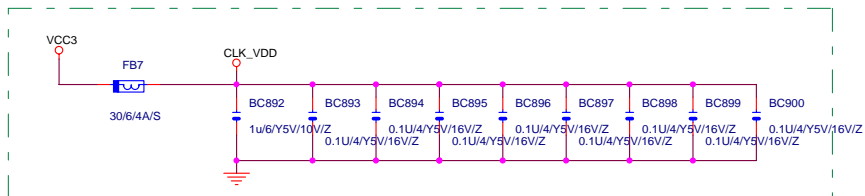
of

39

U3F  
RX780[10HB1-06X780-20R]

Please use 1mm pad size,  
place all ELT test pads  
on bottom side only





- 1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE TO U800 AS POSSIBLE
- 2- ROUTE ALL SRCLKTX AND SRCLKCX AS DIFFERENT PAIR RULE
- 3- PUT DECOUPLING CAPS CLOSE TO U800 POWER PIN

Place R800/801 less than 500 mils away from U800  
R851 less than 100 mils away from R800/801  
route CPU clock as 100ohm differential pair

Parallel Resonance Crystal

watch dog --  
RESTORE# 接 RESET

Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.

U185B  
eGND65 THERMAL GND

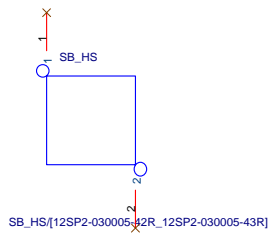


**GIGABYTE**

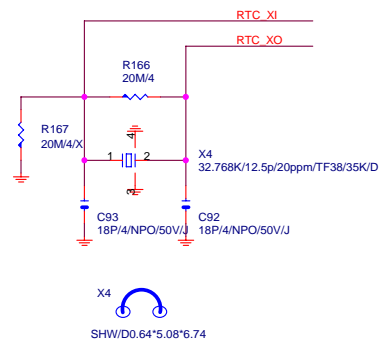
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Size Custom	Document Number <b>GA-MA770T-UD3P</b>	Rev <b>1.1</b>
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S.B HEATSINK

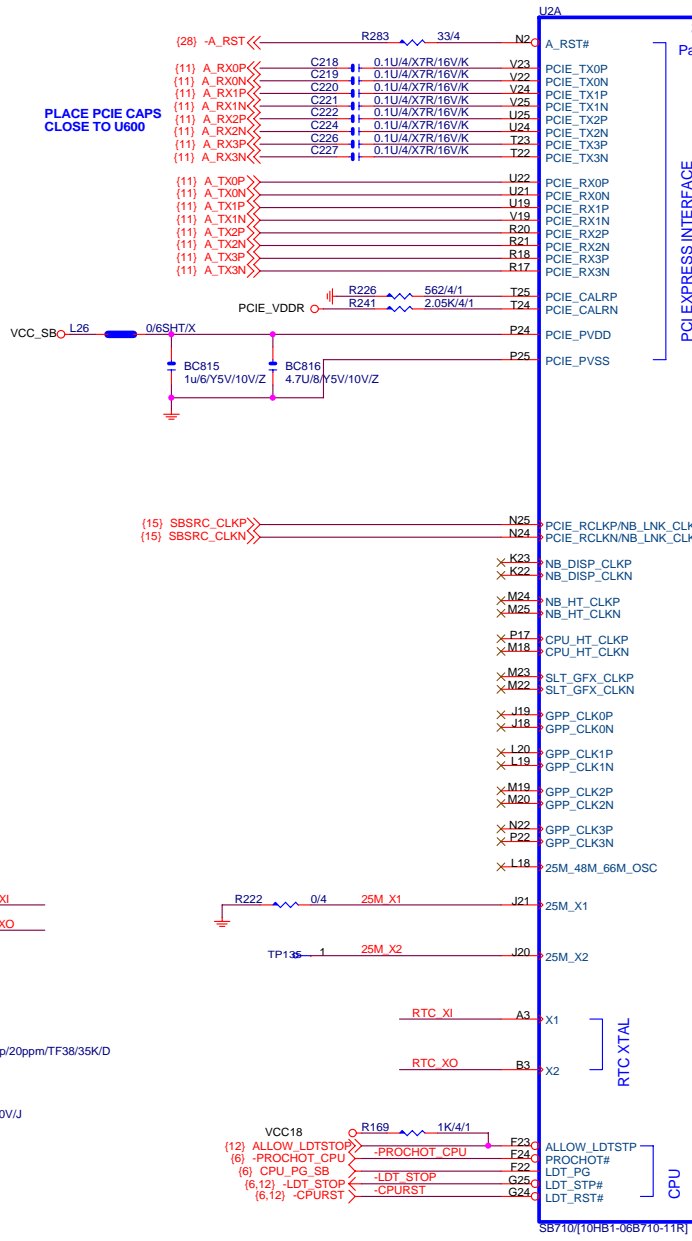


SB\_HS[12SP2-030005;2R\_12SP2-030005-43R]



SHW/D0.64\*5.08\*6.74

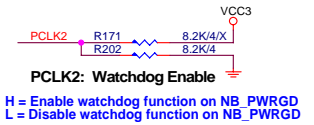
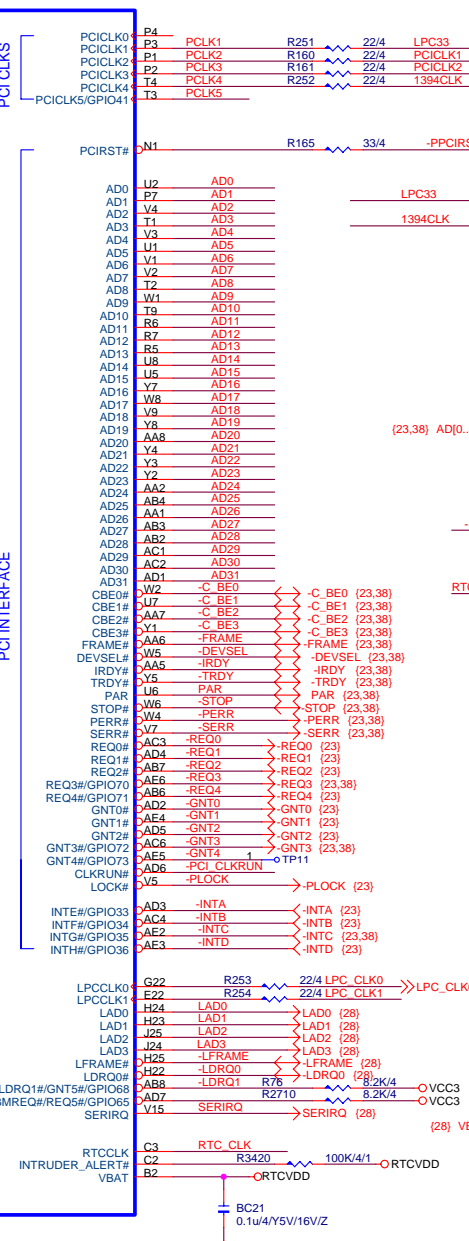
PLACE PCIE CAPS  
CLOSE TO U600



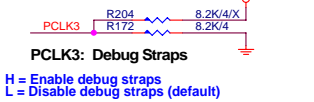
CLR_CMOS	
SHORT	CLEAR CMOS
OPEN	NORMAL

NOT ADD ICT FOR RTCVDD PIN

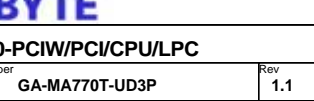
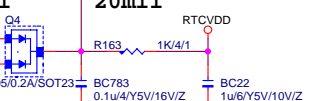
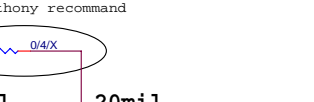
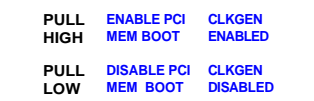
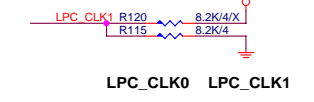
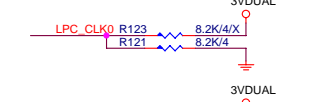
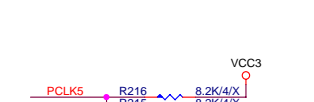
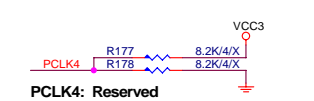
SB700  
Part 1 of 5



H = Enable watchdog function on NB\_PWRGD  
L = Disable watchdog function on NB\_PWRGD



H = Enable debug straps  
L = Disable debug straps (default)

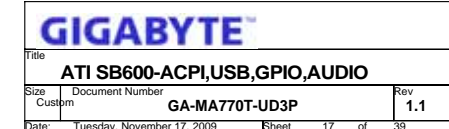


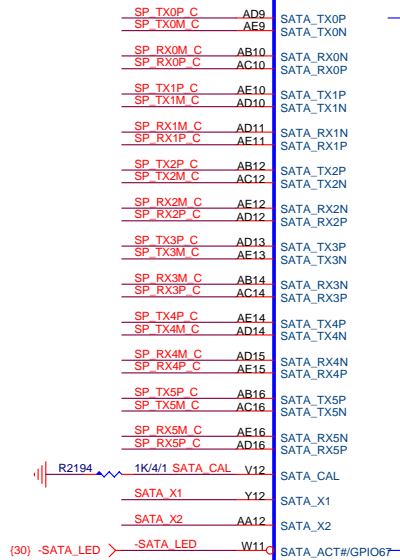
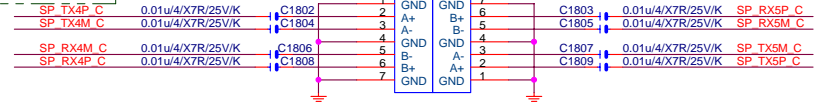
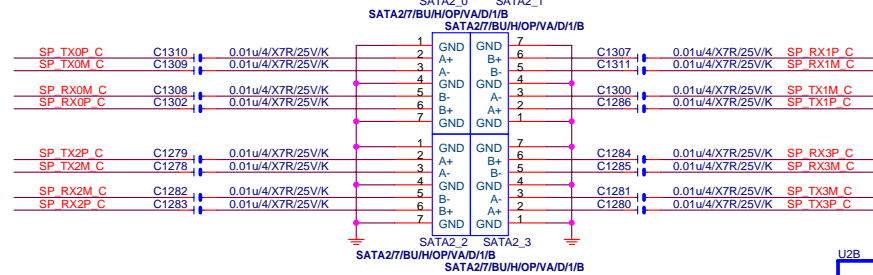
**GIGABYTE**

ATI SB600-PCIW/PCI/CPU/LPC

GA-MA770T-UD3P

Rev 1.1





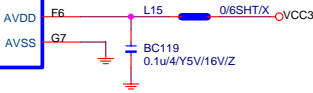
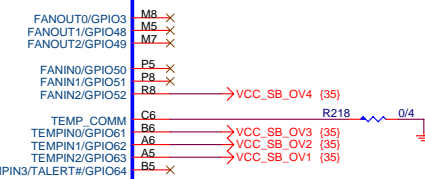
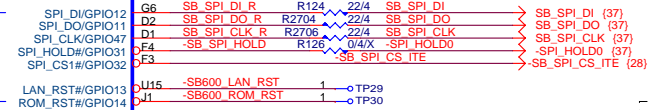
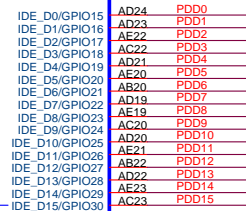
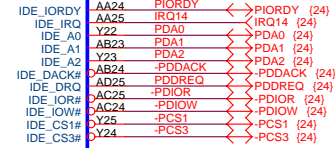
SB700  
Part 2 of 5

SERIAL ATA

ATA 66/100/133

SPI ROM

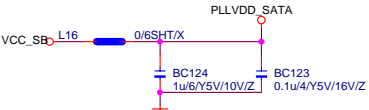
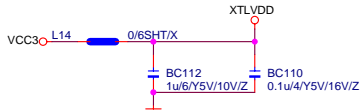
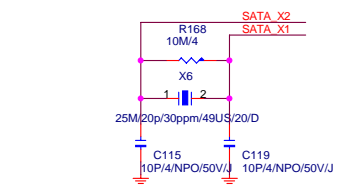
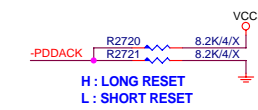
HW MONITOR

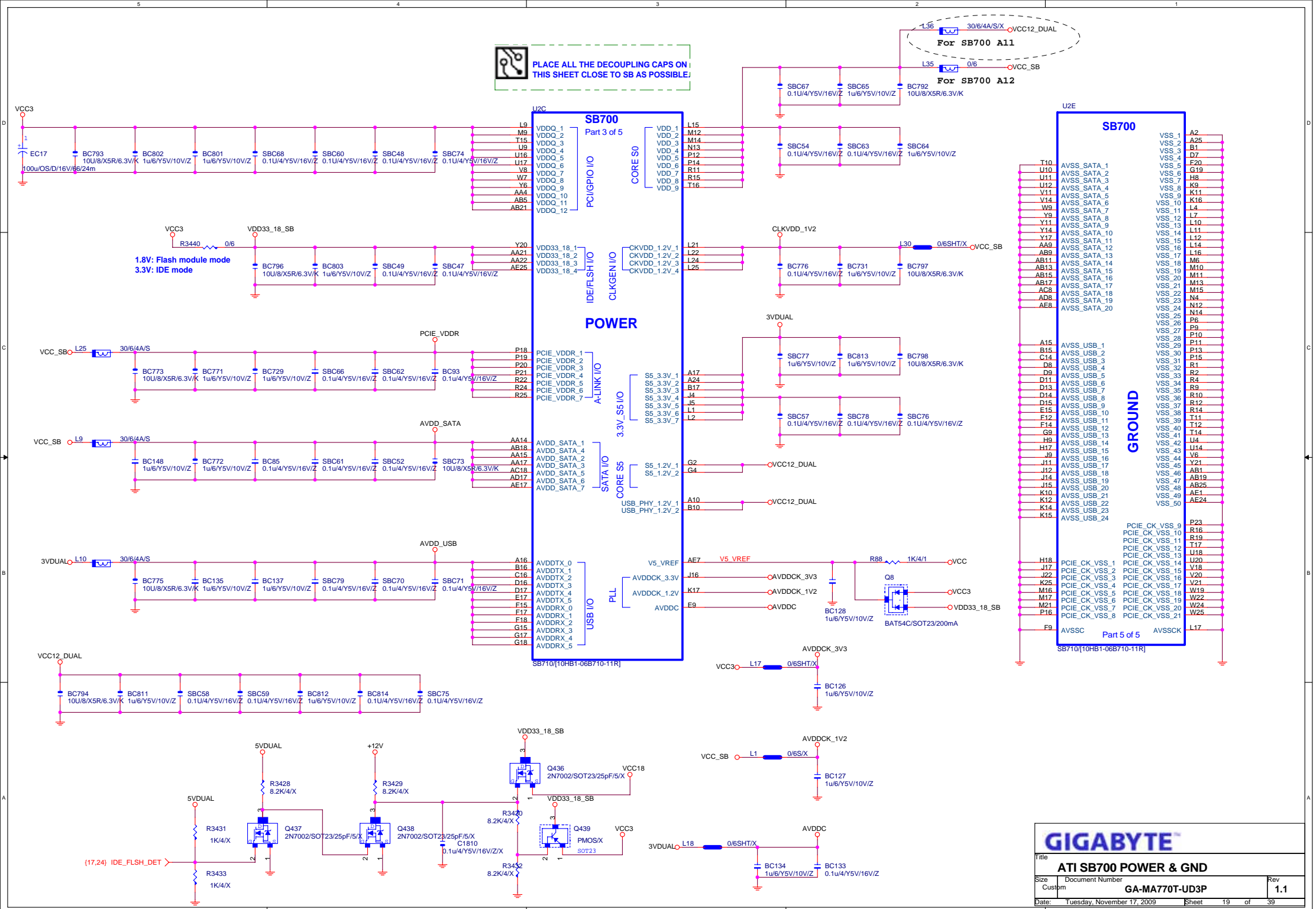


Special NS\_VIA CONNECTS  
HWM\_AGN2 TO GND at VIA  
hole only

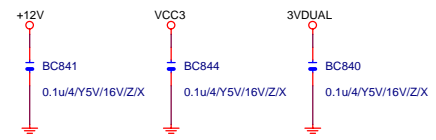
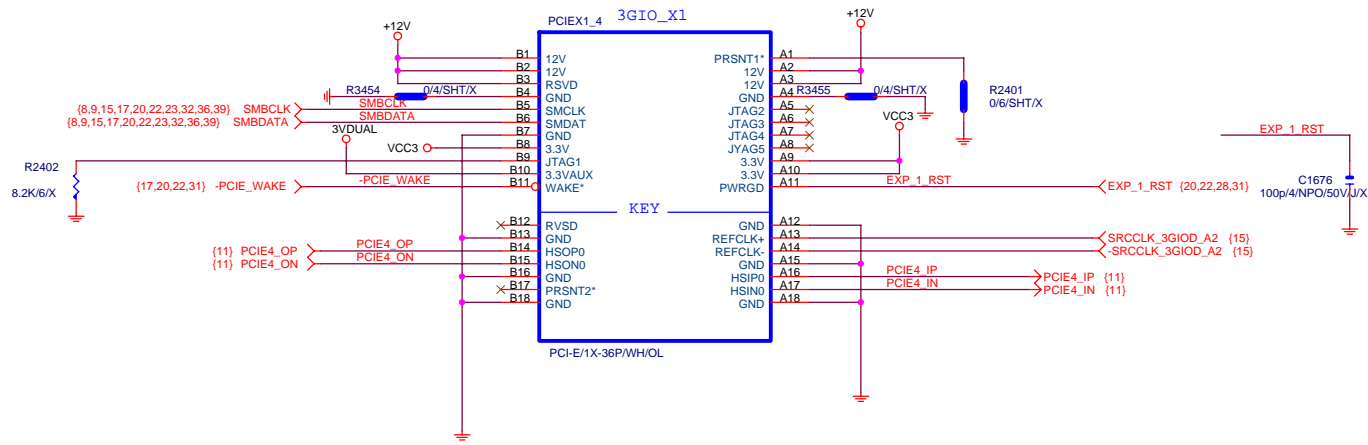


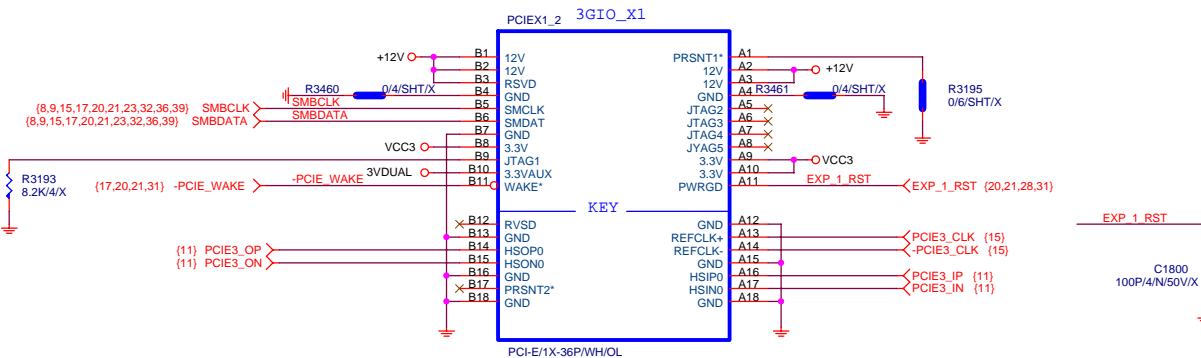
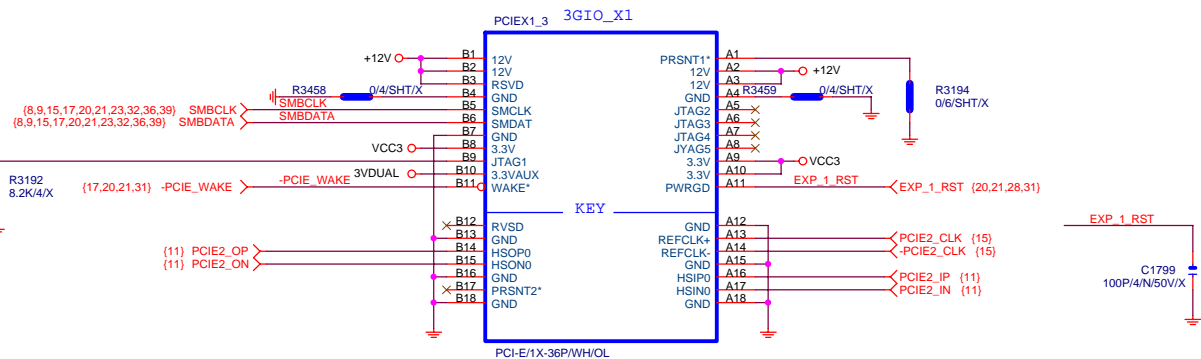
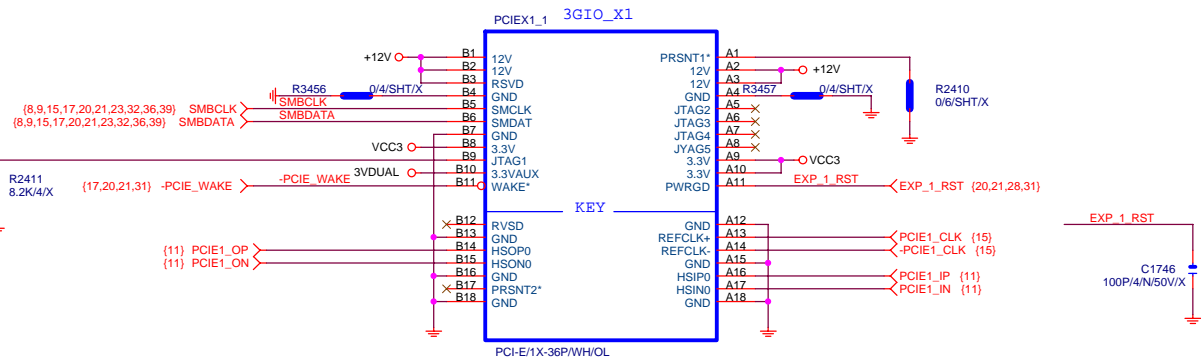
NOTE: ROUTE TEMP\_COMM  
AS A 10MIL TRACE





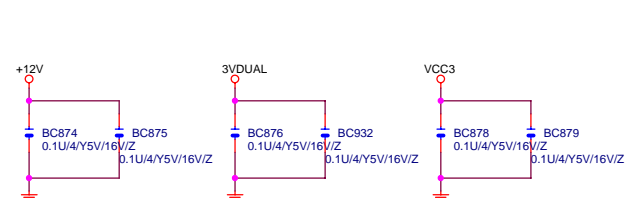
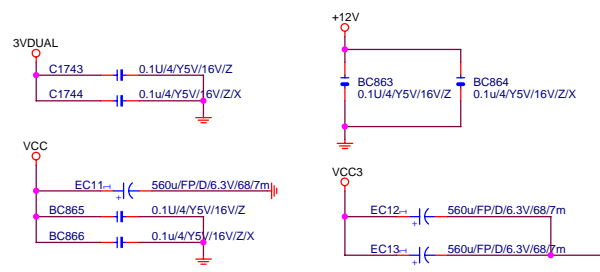
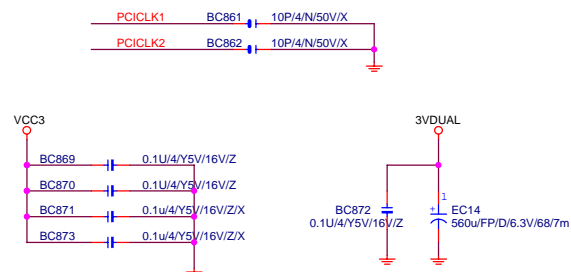
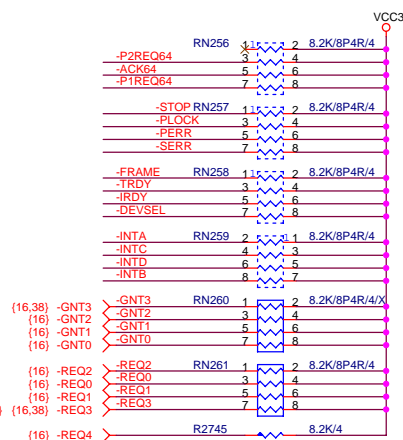
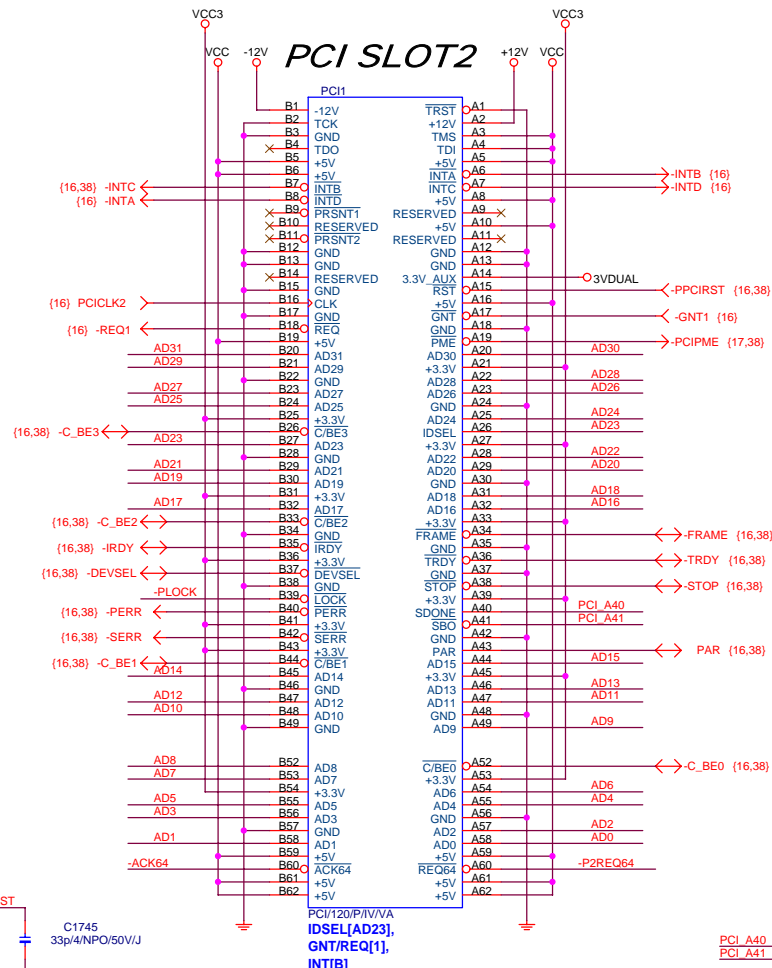
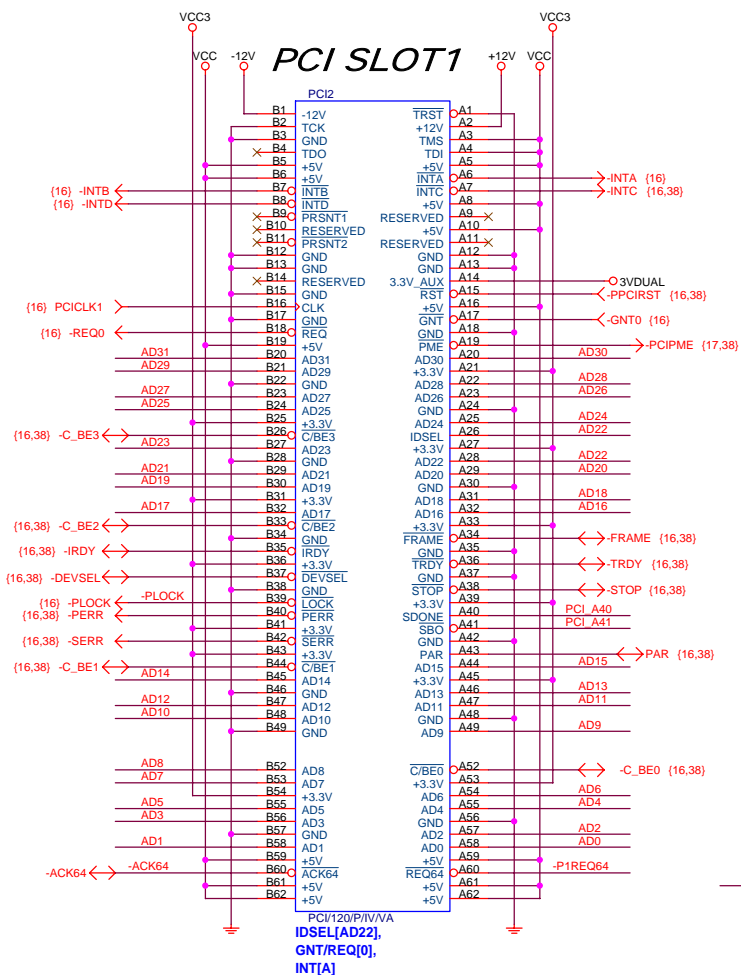


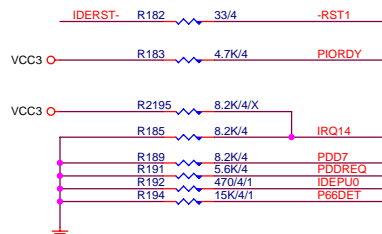
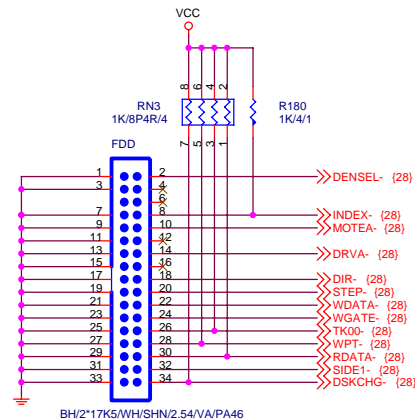




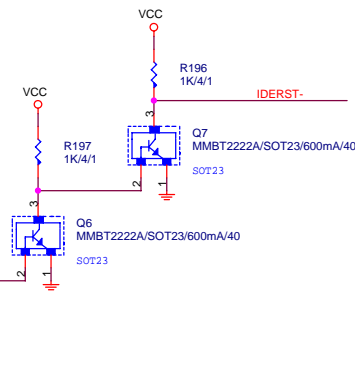
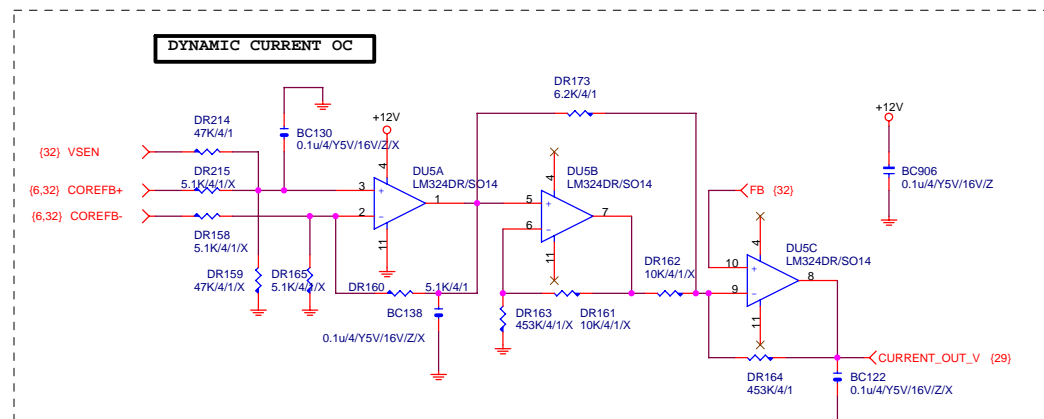
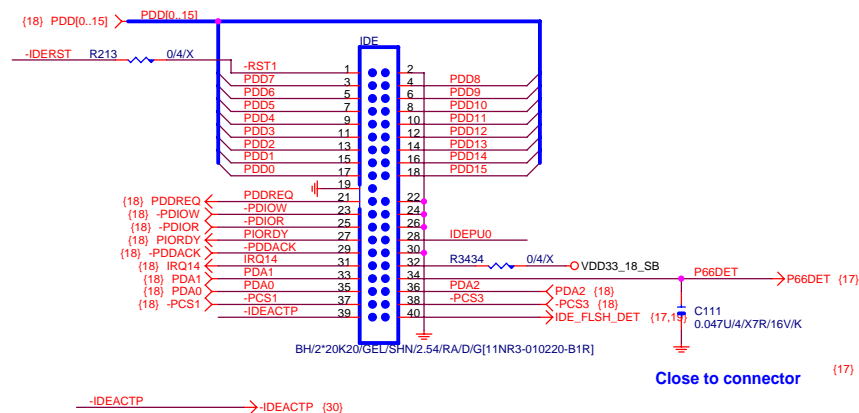


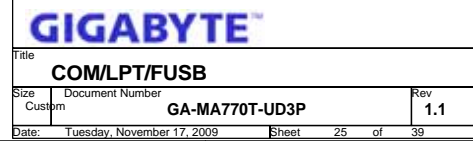
PCI SLOT 1,2
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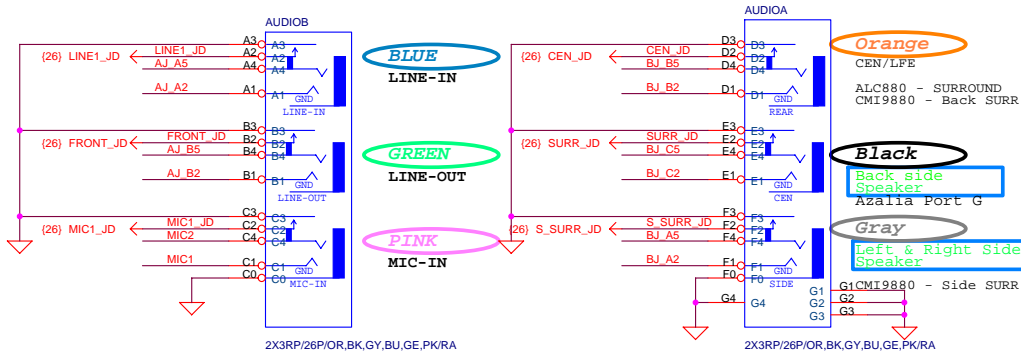
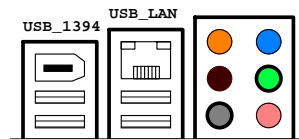
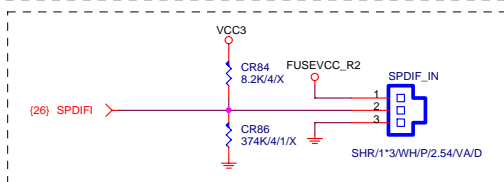
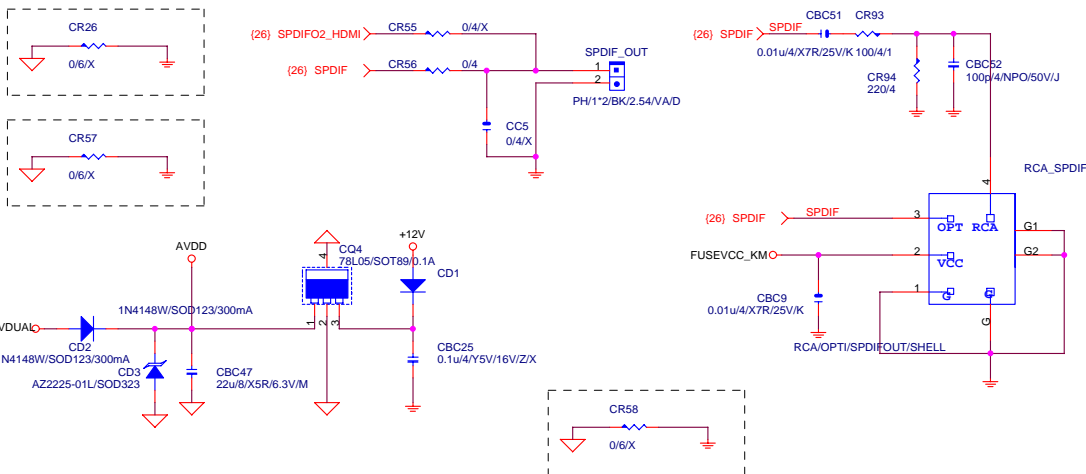


### PRIMARY IDE CONNECTOR

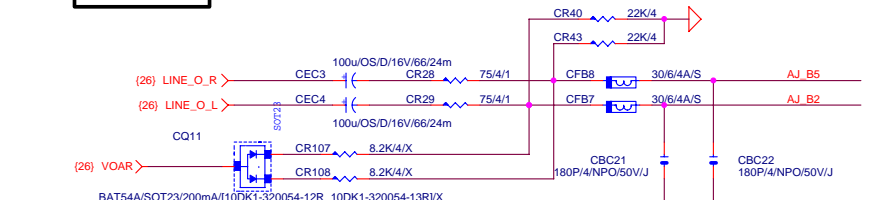




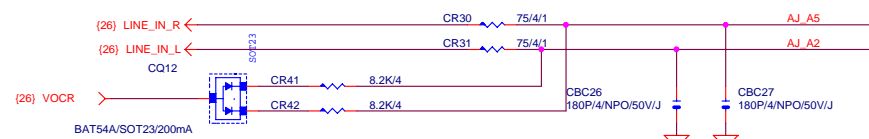




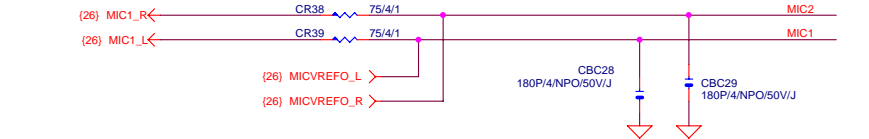
## LINE OUT FRONT OUT



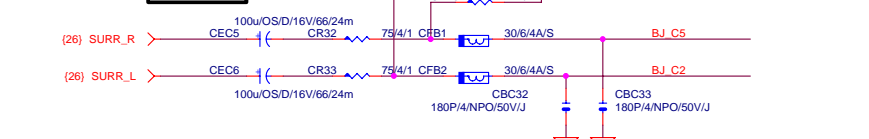
## LINE-IN



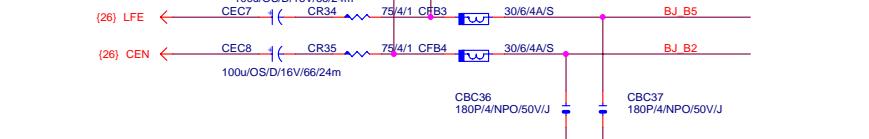
## MIC



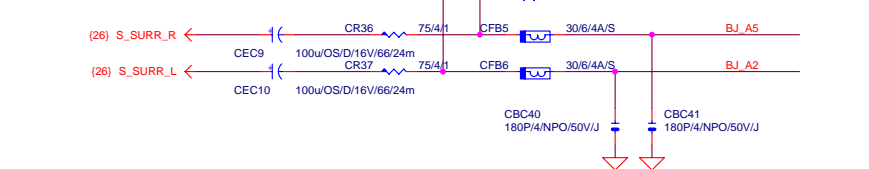
## SURROUND



## CEN/LFE



## SURR BACK



**GIGABYTE**

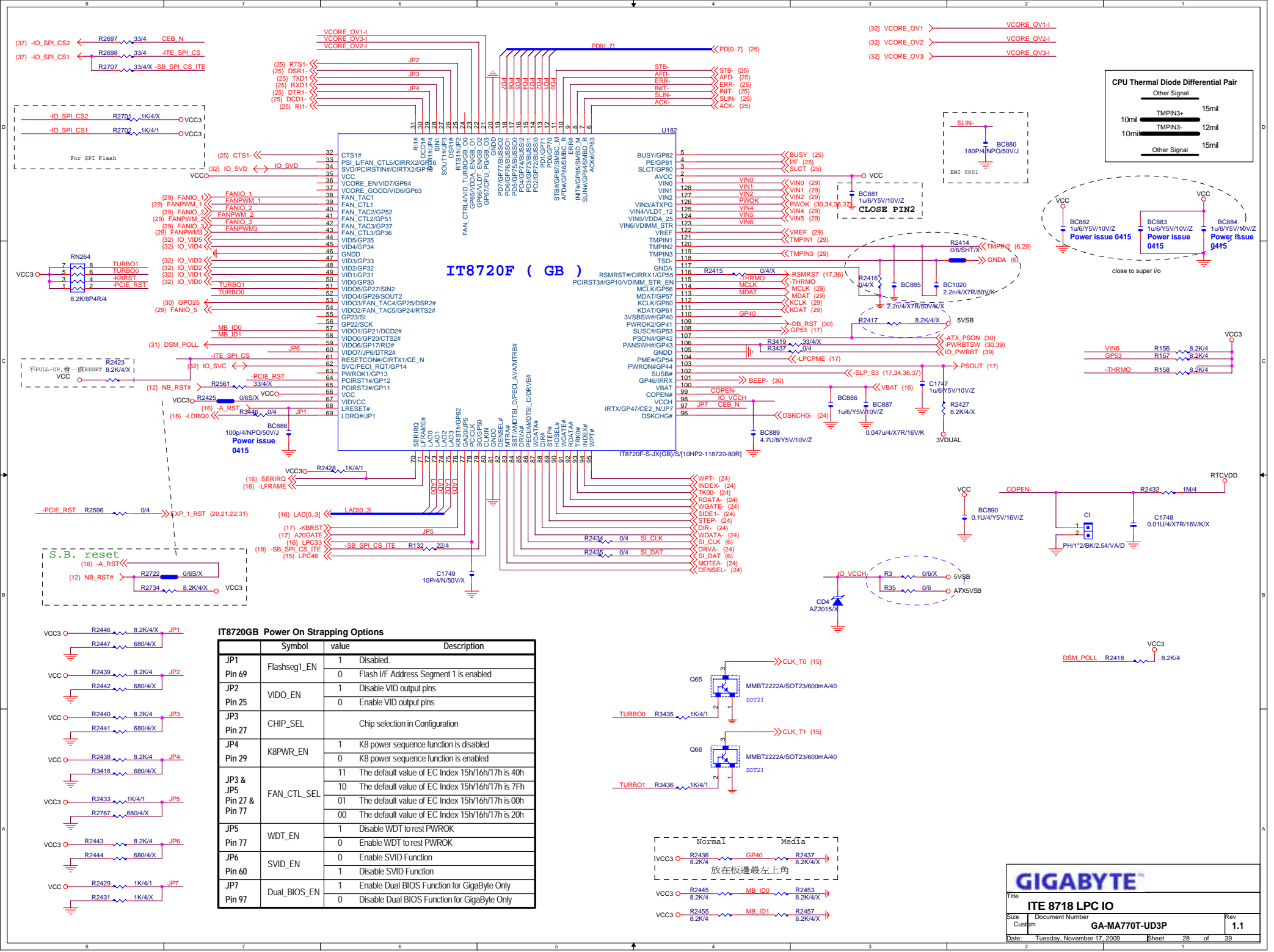
REAR AUDIO JACK

GA-MA770T-UD3P

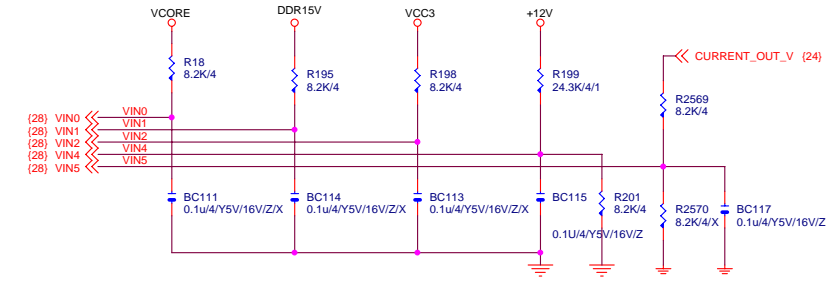
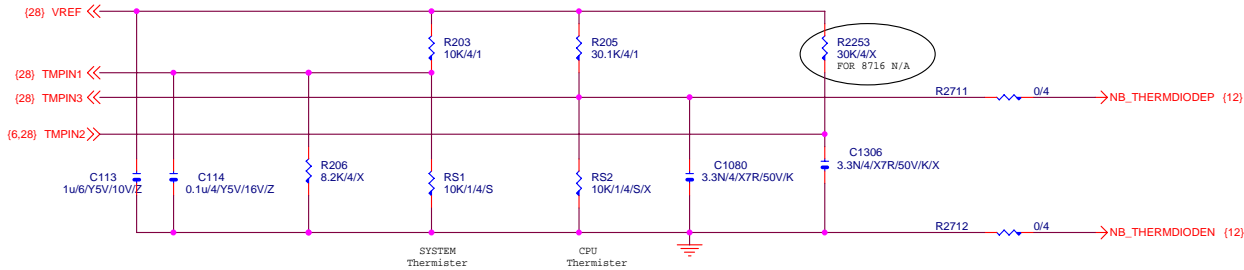
Rev 1.1

Date: Tuesday, November 17, 2009

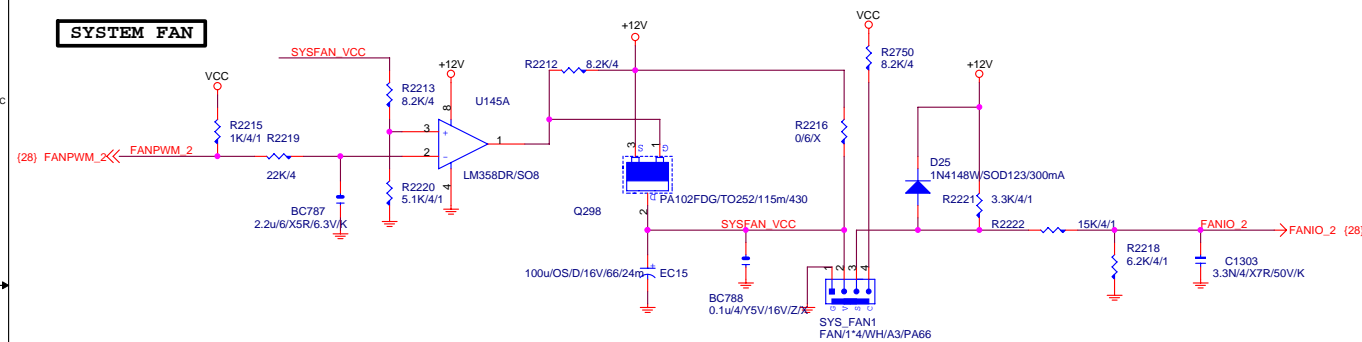
Sheet 27 of 39



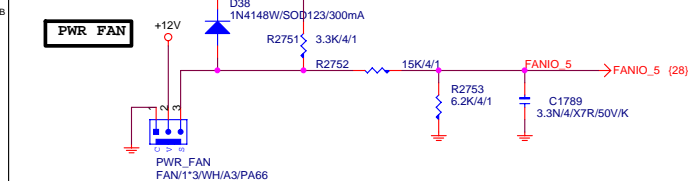
## Hardware Monitor circuits



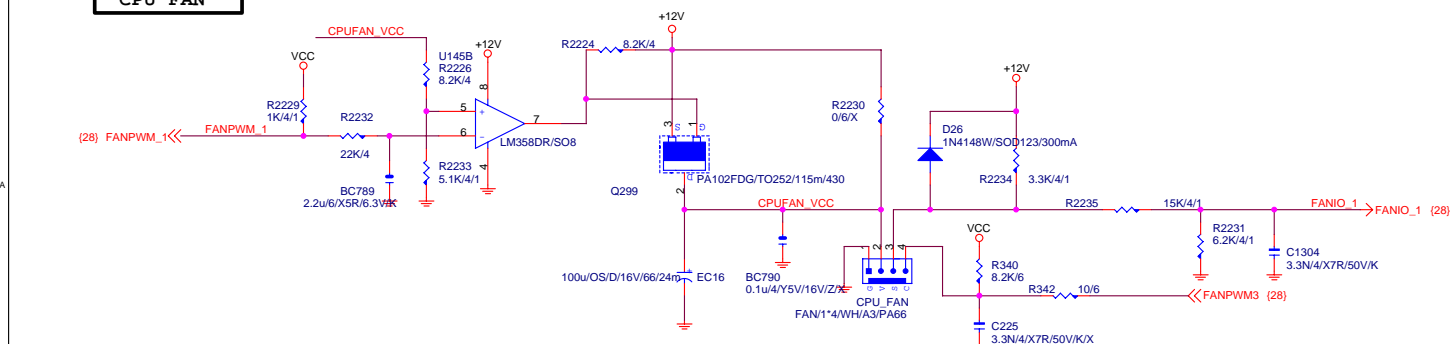
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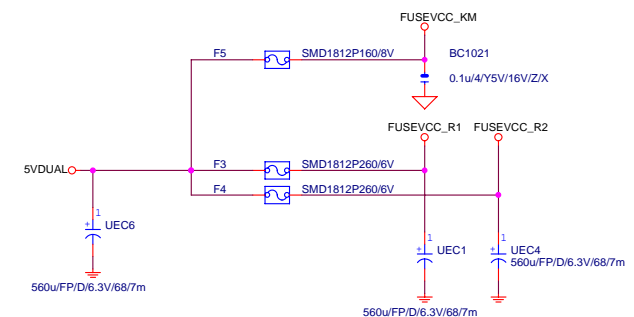
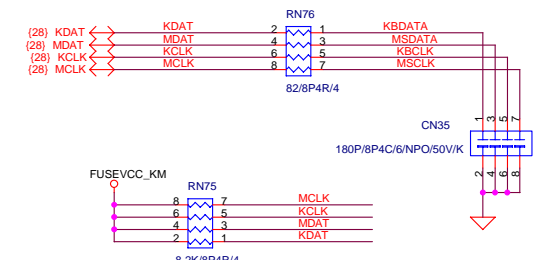
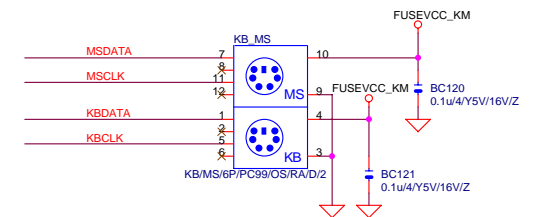
PWR FAN



## CPU FAN



**KB & MS**







# PCIE-1G LAN

EXP 1 RST LBC65 100p/4NPO/50V/J/X

for RT8111B N/C  
for RT8111C 0 ohm  
(Internal Regulator)  
for RT8111C N/C  
(external Regulator)

距離在0.5cm以內

For RT8111C

22u/8/X5R/6.3V/M  
0.1u/4/X7R/16V/K

XTALU P.1

LC2 25M/20p/30ppm/49US/20/D

LC5 27p/4/NPO/50V/J

LC6 27p/4/NPO/50V/J

LC7 27p/4/NPO/50V/J

LC8 27p/4/NPO/50V/J

LC9 27p/4/NPO/50V/J

LC10 27p/4/NPO/50V/J

LC11 27p/4/NPO/50V/J

LC12 27p/4/NPO/50V/J

LC13 27p/4/NPO/50V/J

LC14 27p/4/NPO/50V/J

LC15 27p/4/NPO/50V/J

LC16 27p/4/NPO/50V/J

LC17 27p/4/NPO/50V/J

LC18 27p/4/NPO/50V/J

LC19 27p/4/NPO/50V/J

LC20 27p/4/NPO/50V/J

LC21 27p/4/NPO/50V/J

LC22 27p/4/NPO/50V/J

LC23 27p/4/NPO/50V/J

LC24 27p/4/NPO/50V/J

LC25 27p/4/NPO/50V/J

LC26 27p/4/NPO/50V/J

LC27 27p/4/NPO/50V/J

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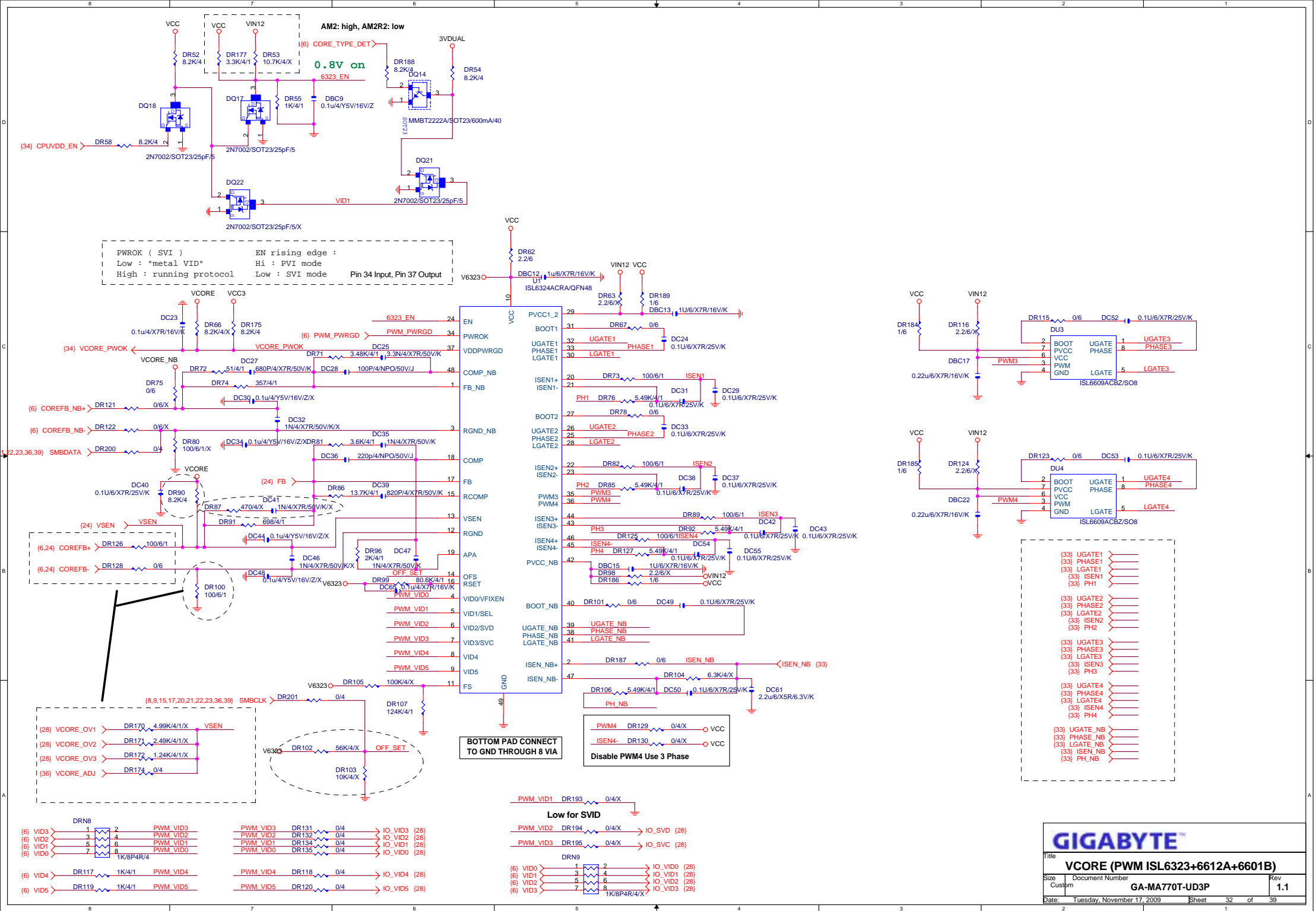
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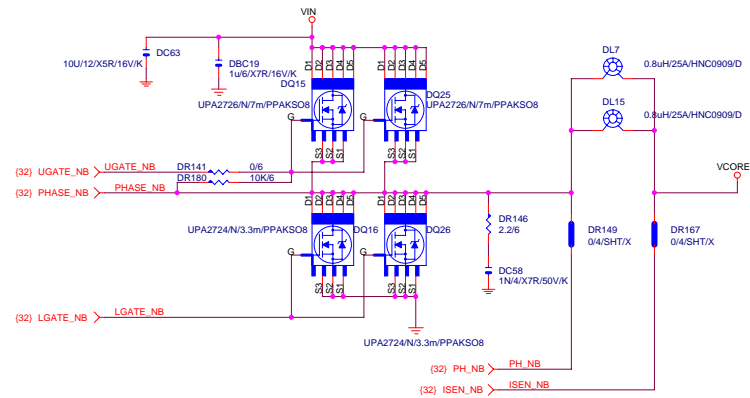
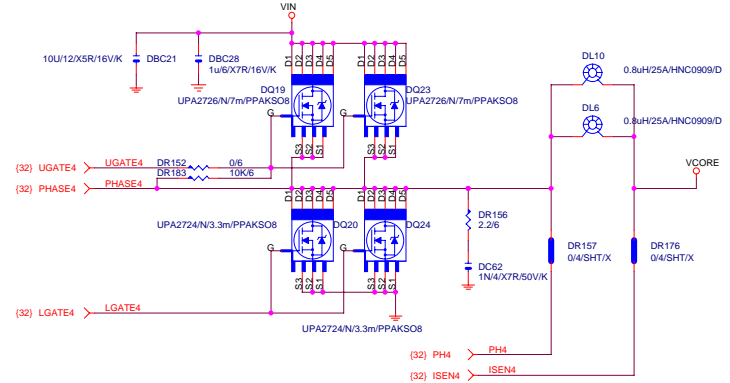
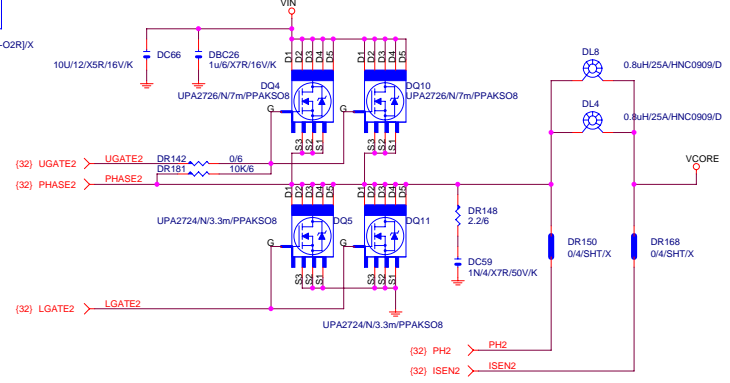
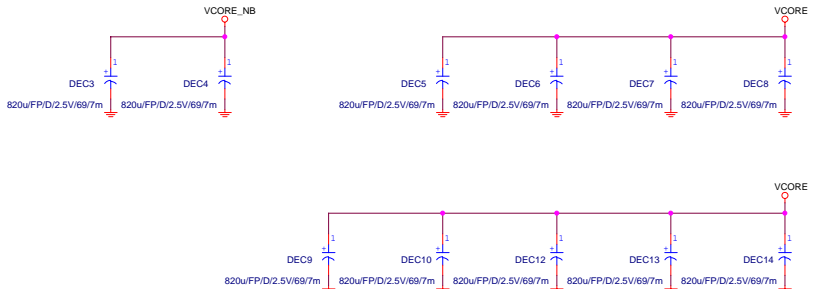
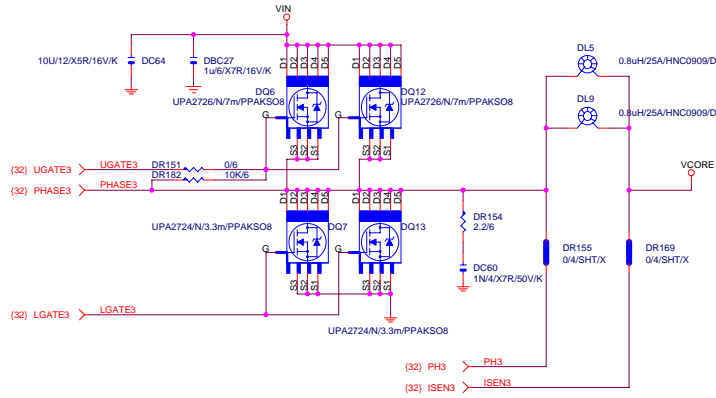
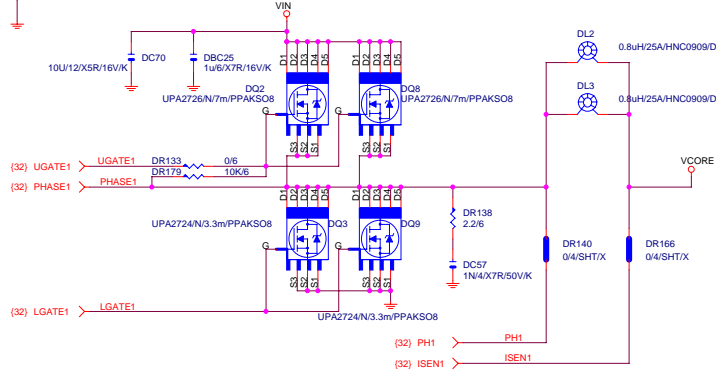
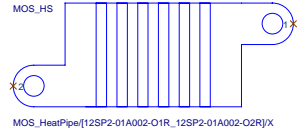
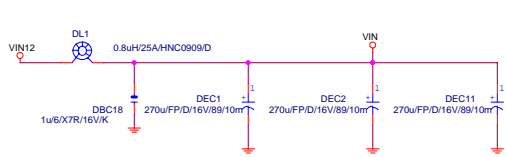
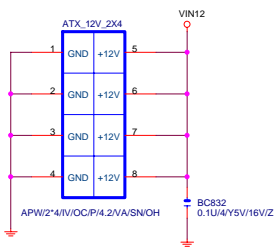
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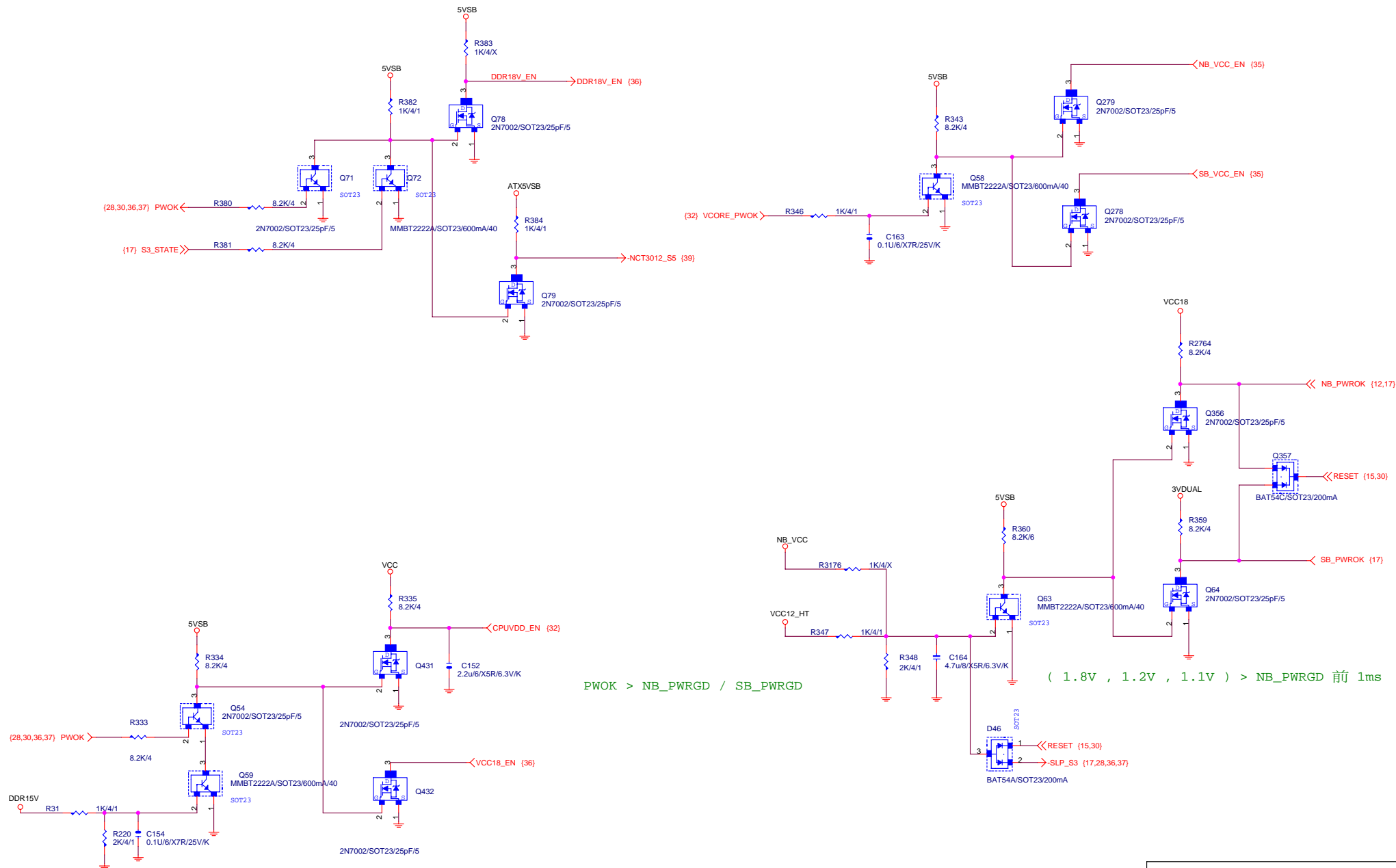
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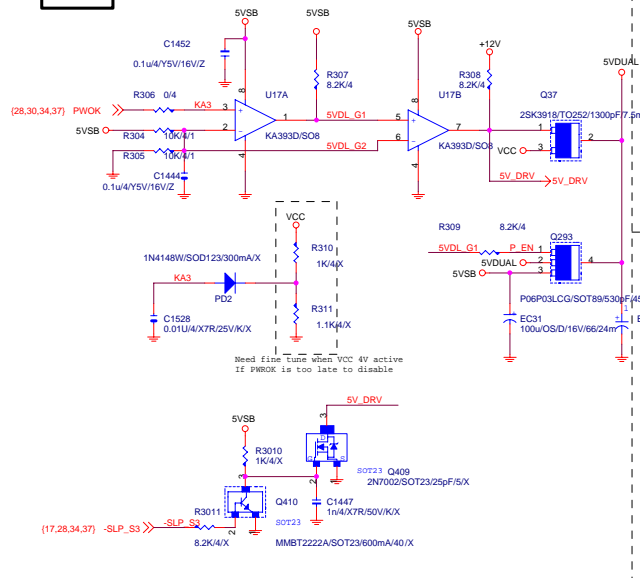


**GIGABYTE**

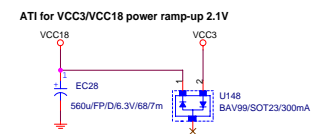
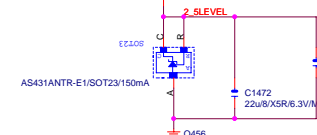
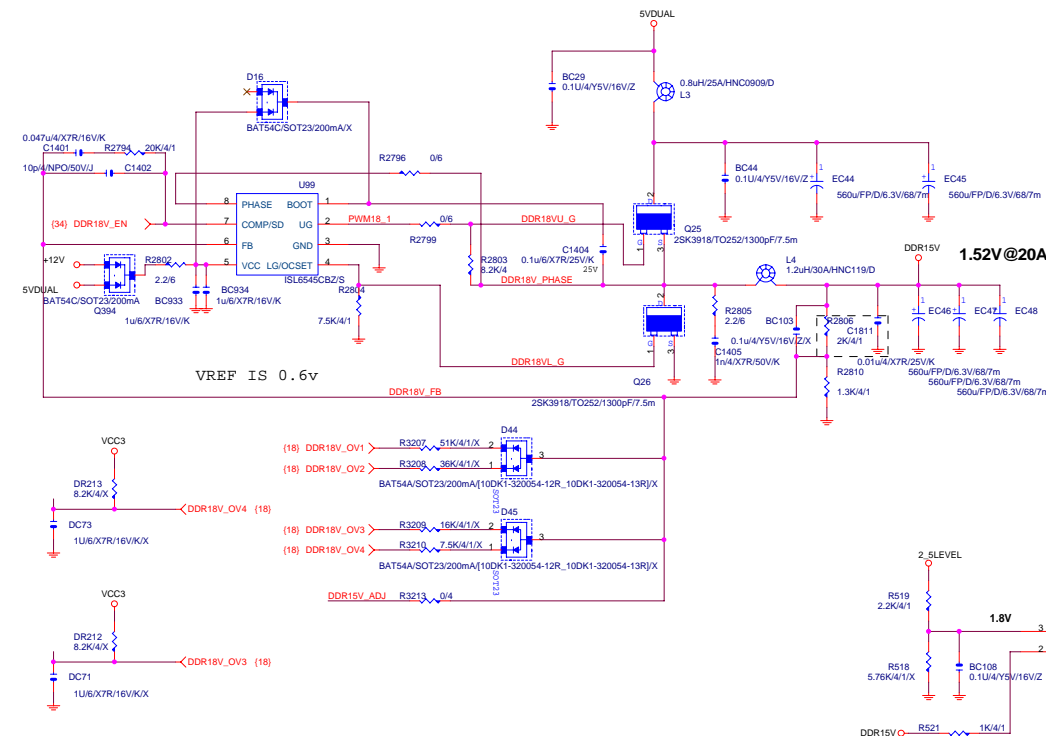
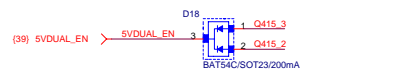
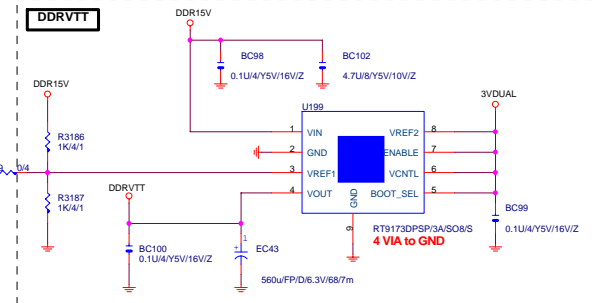
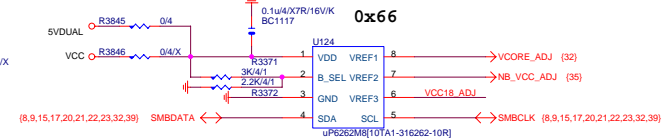
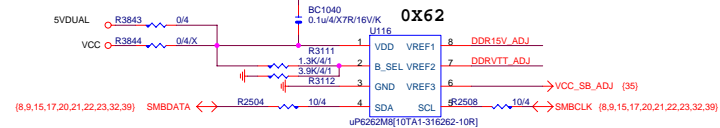
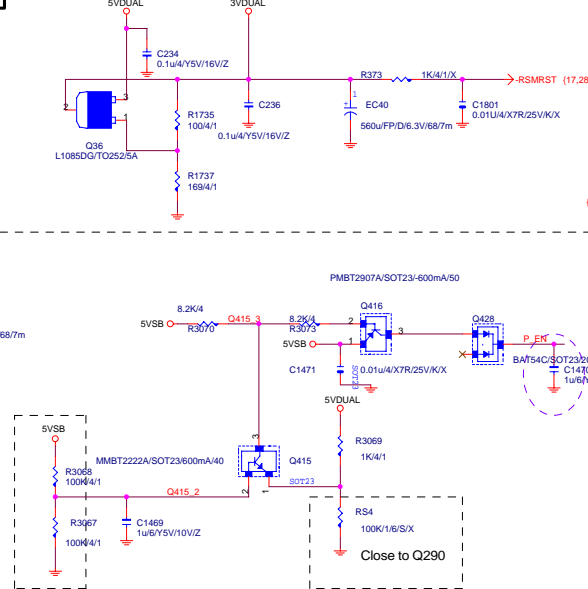




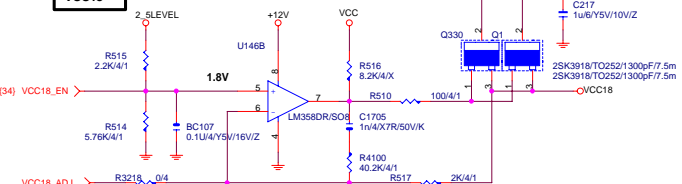
## 5VDUAL



## 3VDUAL



## VCC18

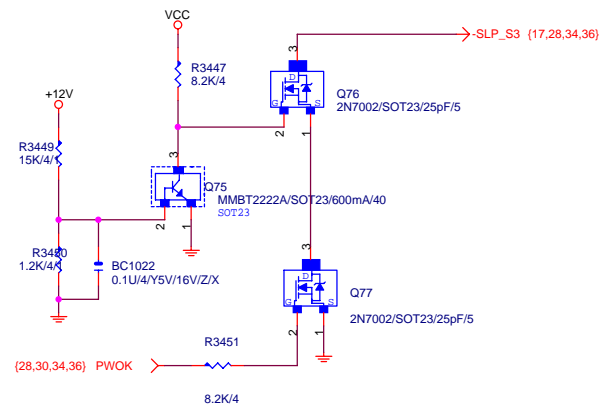
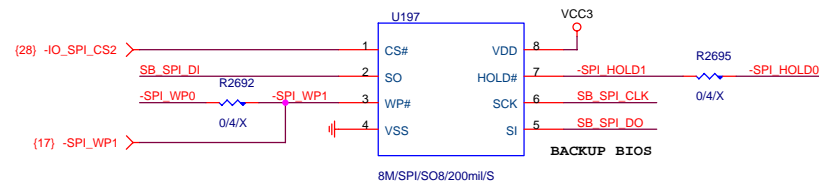
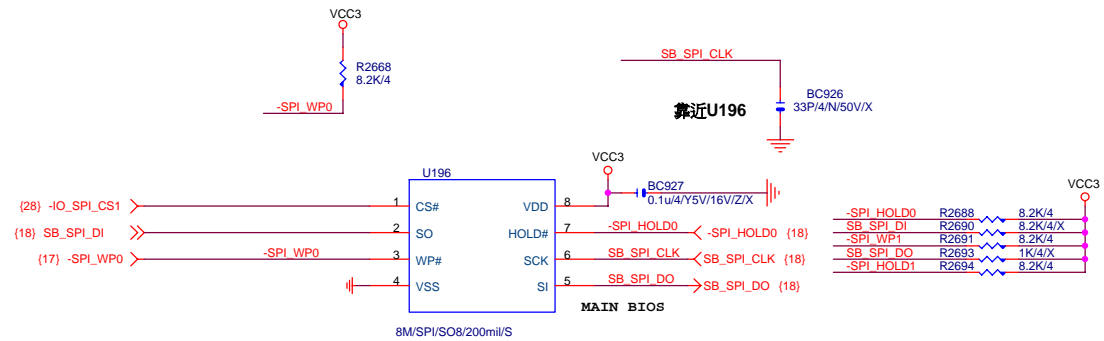


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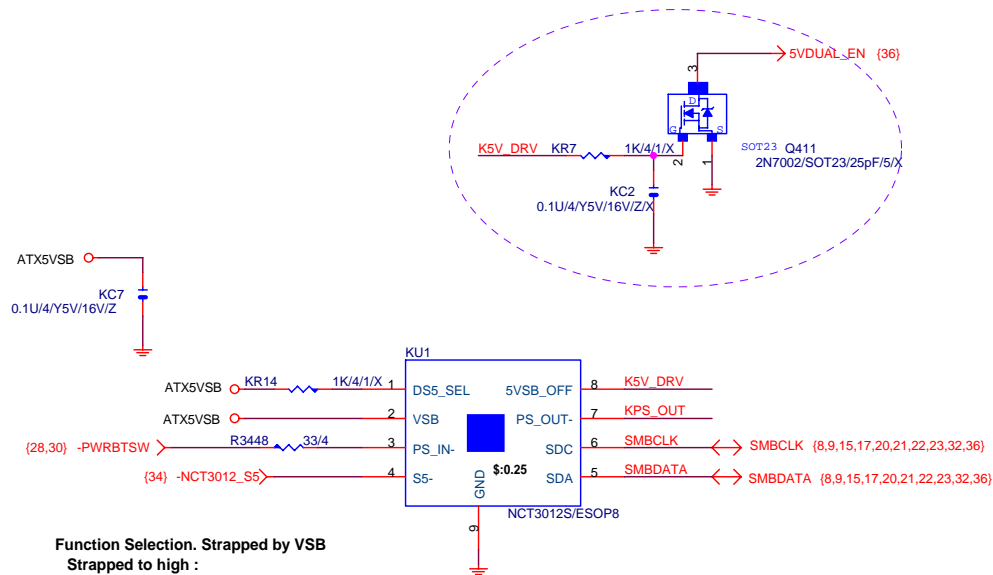
DDR2 POWER, VCC18

File	Document Number	Rev
Size	GA-MA770T-UD3P	1.1
Date	Wednesday, December 16, 2009	Sheet 36 of 39









#### Function Selection. Strapped by VSB

Strapped to high :

DeepS5\_Sel = 1:

System will enter the deep S5 state after 6 sec delays when AC power on.

Strapped to low : (Default)

DeepS5\_Sel = 0:

System will not enter the deep S5 state when AC power on. System is in normal ACPI S5 state.

